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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,025	07/02/2001	Toshiaki Shinohara	210096US2	7453

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EXAMINER
VU, QUANG D

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Acti n Summary	Application No.	Applicant(s)	
	09/895,025	SHINOHARA, TOSHIAKI	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP Patent No. 10-93015 Toshio.

Regarding claim 1, Toshio teaches a semiconductor device comprising:

a semiconductor element having a leadframe (13);

a metal block (19) having a first surface and a second surface opposite to the first surface;

an leadframe (13) joined to the first surface of the metal block; and

a ceramic substrate (18) joined to the second surface of the metal block and having metal layers formed on both surfaces,

wherein the semiconductor element and the leadframe are joined to the first surface of the metal block through a jointing material.

Toshio teaches the leadframe made of copper. Toshio does not teach the electrode terminal. It would have been obvious to one having to one ordinary skill in the art at the time the invention was made to include the electrode terminal, since the leadframe and electrode terminal are used for the interconnection.

Regarding claim 2, Toshio teaches the metal layers formed on the both surfaces of the ceramic substrate (see figures 1 and 4). Toshio does not teach both of metal layer are the same thickness. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have both of metal layers are the same thickness, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. Furthermore, the thickness of both metal layers is disclosed on the Admitted Prior Art.

Regarding claim 3, Toshio teaches the semiconductor element includes a plurality of semiconductor elements; the metal block and the ceramic substrate are separated per insulation unit of at least one of the plurality of semiconductor elements; one of the metal block and the ceramic substrate is provided to be in corresponding to at least one of the plurality of semiconductors elements; and another one of the metal block and the ceramic substrate extends over all of the plurality of semiconductor elements for forming the insulation unit (see figure 1).

Regarding claim 4, Toshio teaches the metal block (19) includes a surface having a region larger than that of the jointing material (12) on a side opposite to the jointing material (see figure 1).

Regarding claim 5, Toshio teaches a gap between the metal block (19) and the semiconductor element (11) and the gap is filled with the jointing material (see figure 1). Toshio does not teach a gap becomes wider as a distance from a center of the semiconductor element becomes longer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal gap, since the solder or resin material is a known material.

3. Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP Patent No. 10-93015 Toshio in view of JP Patent No. 2001-118961 to Takagi.

Regarding claim 6, Toshio teaches a semiconductor device comprising:

a metal block (19) having a first surface and s second surface opposite to the first surface;

a semiconductor element (11) joined to the first surface of the metal block through a jointing material (12);

a resin package (17) for sealing the metal block and the semiconductor element,

Toshio does not teach a resin insulating layer having a third surface and a fourth surface opposite to the third surface, the third surface being joined to the second surface of the metal block; and wherein the fourth surface of the resin insulating layer is exposed, and the resin insulating layer has an elasticity higher than that of the resin package. However, Takagi teaches the resin film (see figures 1 and 5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Takagi into the device taught by Toshio, since the resin layer can be used as an adhesive material. If the teaching of Takagi had been incorporated into the device taught by Toshio, a resin insulating layer will be formed under the metal block and will have a third surface and a fourth surface opposite to the third surface, the third surface being joined to the second surface of the metal block; and wherein the fourth surface of the resin insulating layer is exposed, and the resin insulating layer has an elasticity higher than that of the resin package.

Regarding claim 7, Toshio does not teach the resin insulating layer is made of a silicon resin including a ceramic material for filling the silicon resin. However, Takagi teaches the resin insulating layer is made of a silicon resin including a ceramic material for filling the silicon

resin. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Takagi into the device taught by Toshio, since the silicon resin including a ceramic material is commonly used for filling the silicon resin.

Regarding claim 8, Toshio teaches the metal block is provided per insulation unit of the semiconductor element (see figures 1-4).

Regarding claim 9, Toshio teaches the metal block includes a surface having a region larger than that of the jointing material on a side opposite to the jointing material (see figures 1 and 2).

Regarding claim 10, Toshio teaches a gap between the metal block (19) and the semiconductor element (11) and the gap is filled with the jointing material (see figure 1). Toshio does not teach a gap becomes wider as a distance from a center of the semiconductor element becomes longer. It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal gap, since the solder or resin material is a known material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QVU
July 15, 2002

Sara Crane
Primary Examiner